



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,629	03/03/2004	Soo-Chan Lee	2421-000033/US	3096

7590 10/03/2006

HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 8910
RESTON, VA 20195

EXAMINER

HOLLINGTON, JERMELE M

ART UNIT	PAPER NUMBER
----------	--------------

2829

DATE MAILED: 10/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/791,629

Applicant(s)

LEE ET AL.

Examiner

Jermele M. Hollington

Art Unit

2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 July 2006.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-34 and 37-42 is/are pending in the application.
- 4a) Of the above claim(s) 11-32, 38 and 39 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10, 33, 34, 37 and 40-42 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-10, 33-34, 37 and 40-42 are rejected under 35 U.S.C. 102(b) as being anticipated by Kobayashi et al (6384593).

Regarding claim 1, Kobayashi et al disclose [see Figs. 1-2] a semiconductor device test apparatus comprising a main body (combination of sections 200, 300 and 400) including a loading robot (movable head 303 and movable arm 302) and a sorting robot (movable head 403) disposed thereon, and an unloading robot (movable arm 402) disposed thereon and adapted to [see Note] move along X-axis and Y-axis; a soak chamber (temperature chamber 101), a test chamber (102); a desoak chamber (temperature stress removing chamber 103); wherein the soak chamber (101), the test chamber (102), and the desoak chamber (103) are attached to the main body (200, 300, 400 see Figs. 4-5) and adapted to [see Note] be separated from the main body (200, 300, and 400).

Regarding claim 2, Kobayashi et al disclose the soak chamber (101), the test chamber (102), and the desoak chamber (103) are adapted to be [see Note] separated from the main body (200, 300 and 400) using a sliding unit.

Regarding claim 3, Kobayashi et al disclose a semiconductor device test apparatus comprising: a main body (combination of sections 200, 300 and 400) including a loading robot

Art Unit: 2829

(movable head 303 and movable arm 302) and a sorting robot (movable head 403) disposed thereon, and an unloading robot (movable arm 402) disposed thereon and adapted to [see Note below] move along X-axis and Y-axis; and a stacker (transfer means 304 and 404) for stacking devices (ICs) before and after a test, the stacker (304 and 404) including user trays (test trays TST) for stacking the devices (ICs), wherein the user trays (TST) are adapted to [see Note] be interchangeable such that the user trays (TST) may be being used to stack the devices (ICs) prior to the test and to stack the devices (ICs) after the test.

Regarding claim 4, Kobayashi et al disclose the user trays (TST) are adapted to be interchanged in accordance with the process of the test.

Regarding claim 5, Kobayashi et al disclose a semiconductor device test apparatus comprising: a main body (combination of section 200, 300 and 400) including a loading robot (movable head 303 and movable arm 302) and a sorting robot (movable head 403) disposed thereon, and an unloading robot (movable arm 402) disposed thereon and adapted to [see Note] move along X-axis and Y-axis; a stacker (transfer means 304 and 404) for stacking devices (ICs) before and after a test, the stacker (304 and 404) including at least one user tray feeder (means 304) predesignated with a function for stacking un-tested devices (ICs) and at least one user tray sender (means 404) predesignated with a function, for stacking tested devices (ICs), wherein the user tray (test tray TST) functions being adapted [see Note] to be interchangeable during stacker operation.

Regarding claim 6, Kobayashi et al disclose a semiconductor device test apparatus comprising: a main body (combination of sections 200, 300 and 400) including a loading robot (movable head 303 and movable arm 302) and a sorting robot (movable head 403) disposed

Art Unit: 2829

thereon, and an unloading robot (movable arm 402) disposed thereon and adapted to [see Note below] move along X-axis and Y-axis; and a stacker (transfer means 304 and 404) arranged in the main body (200, 300 and 400), the stacker (304 and 404) having a user tray feeder (means 304) which loads a plurality of user trays (test TST) having a desired quantity of devices (ICs) to be tested and a user tray sender (means 404) which loads the plurality of user trays (TST) having the devices sorted by their grades in accordance with the test result, the user tray feeder (304) and the user tray sender (404) adapted to [see Note] be interchanged in their uses in accordance with the process of the test.

Regarding claim 7, Kobayashi et al disclose a soak chamber (temperature chamber 101) for receiving the test tray (TST) inputted from the device loader (loader section 300), and for preheating or precooling the devices (ICs); a test chamber (102) for connecting the preheated devices (ICs) in the soak chamber (101) to a socket of a test head (tester head 104) and for performing a test; a desoak chamber (stress removing chamber 103) for receiving the test tray (TST) discharged from the test chamber (102) and for discharging them to a device unloader (unloader section 400) after recovering them to a room temperature, wherein the soak chamber (101), the test chamber (102) and the desoak chamber (103) are adapted to [see Note] be separated from the main body (200, 300 and 400) using a sliding unit.

Regarding claim 8, Kobayashi et al disclose the soak chamber (101) and the test chamber (102) are made of one body (chamber section 100) to be separated in the same direction.

Regarding claim 9, Kobayashi et al disclose the desoak chamber (103) is adapted to [see Note] be able to be separated in same direction as the separation direction of the soak chamber (101) and the test chamber (102).

Regarding claim 10, Kobayashi et al disclose a loading robot (movable head 303 and movable arm 302) for picking up devices (ICs) to be tested, which are in a stand-by status in the user tray feeder (304) and mounting them on a test tray (TST) being on a device loading stage (300); a sorting robot (movable head 403) for picking up the device discharged to the device unloader (400) and for carrying them to a plurality of sorter tables (storage rack 201) in accordance with the test result; and an unloading robot (movable arm 402) for picking up the device carried to the sorter table (201) and for carrying them to the user tray sender (404).

Regarding claim 33, Kobayashi et al disclose a semiconductor device test apparatus comprising a loading robot (movable head 303 and movable arm 302) for picking up devices (ICs) to be tested, which are in a stand-by status in the user tray feeder (304) and mounting them on a test tray (TST) being on a device loading stage (300); a sorting robot (movable head 403) for picking up the device discharged to the device unloader (400) and for carrying them to a plurality of sorter tables (storage rack 201) in accordance with the test result; and an unloading robot (movable arm 402) for picking up the device carried to the sorter table (201) and for carrying them to the user tray sender (404), and the unloading robot (402) adapted to [see Note] move along an X-axis and Y-axis, wherein the operating speed of the loading robot (302 and 303), the sorting robot (403) and the unloading robot (402) is determined based on the speed of testing the device (ICs).

Regarding claim 34, Kobayashi et al disclose at least one robot (304) used in a test that receives control signals instructing the at least one robot (302 and 303) to carry a device (ICs) at a calculated speed, the calculated speed corresponding based on a time of test execution.

Regarding claim 37, Kobayashi et al disclose a method for stacking devices (ICs) in a semiconductor test apparatus comprising, predesignating at least one user tray feeder (means 304) for stacking un-tested devices, predesignating at least one user tray sender (means 404) for stacking tested devices, designating at least one user tray feeder (304) for stacking tested devices based on the test; stacking at least one tested device (ICs) on the at least one user tray feeder (304).

Regarding claim 40, Kobayashi et al disclose a method for controlling a robot speed of a semiconductor device test apparatus, comprising the steps of: sending control signals to at least one robot (means 304) to carry a device (ICs) for a test detecting a time for the test; calculating a desired speed value of the robot (304) corresponding to the test time detected, and informing the corresponding robot (304) of the calculated speed value to control the speed of the robot (304).

Regarding claim 41, Kobayashi et al disclose the time for the test begins when the device (ICs) contacts a test head (tester head 104) and ends when the device (ICs) is released from the socket.

Regarding claim 42, Kobayashi et al disclose the step of detecting the time for the test includes retrieving stored values of pretested, like kind devices.

Conclusion

3. Applicant's arguments filed July 12, 2006 have been fully considered but they are not persuasive.

Note: claims 1-7 and 9 have the limitation "adapted to" in the claims. MPEP 2111.04 states that claim limitation that employ phrase of the type "adapted to" are typical limitation, which may not distinguish over the prior art. It has been held that the recitation that an element is

Art Unit: 2829

“adapted to” perform a function is not a positive limitation but only requires the ability to so perform.

Furthermore, the examiner disagrees that a soak chamber, a test chamber and a desoak chamber is not separate from the main body. In Figs. 1-2 it shows the above item inside chamber 100, which is not attached to the other main parts of the testing apparatus. Also Figs. 4-5 shows the above items are attached to the other main parts of the testing apparatus.

Since the examiner is maintaining the prior art, the following is applied.

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Since this application has been made final the following is applied.

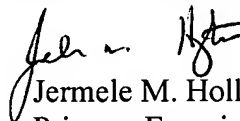
5. This application contains claims 11-32, 38 and 39 drawn to an invention nonelected with traverse in Paper No. 20060124. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Art Unit: 2829

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:00 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


Jermele M. Hollington
Primary Examiner
Art Unit 2829

JMH
September 28, 2006